Amendments to the Specification:

Please replace the paragraph beginning on page 1, with the following rewritten paragraph:

-- The present invention is related to the following applications entitled "Method and Apparatus for Counting Instruction Execution and Data Accesses", serial no. [[_____]] 10/675,777, attorney docket no. AUS920030477US1, filed on September 30, 2003; "Method and Apparatus for Selectively Counting Instructions and Data Accesses", serial no. [[_____]] 10/674,604, attorney docket no. AUS920030478US1, filed on September 30, 2003; "Method and Apparatus for Generating Interrupts Upon Execution of Marked Instructions and Upon Access to Marked Memory Locations", serial no. [[_____]] 10/675,831, attorney docket no. AUS920030479US1, filed on September 30, 2003; "Method and Apparatus for Counting Data Accesses and Instruction Executions that Exceed a Threshold", serial no. [[_____]] 10/675,778, attorney docket no. AUS920030480US1, filed on September 30, 2003; "Method and Apparatus for Counting Execution of Specific Instructions and Accesses to Specific Data Locations", serial no. [[_____]] 10/675,776, attorney docket no. AUS920030481US1, filed on September 30, 2003; "Method and Apparatus for Debug Support for Individual Instructions and Memory Locations", serial no. [[_____]] 10/675,751, attorney docket no. AUS920030482US1, filed on September 30, 2003; "Method and Apparatus to Autonomically Select Instructions for Selective Counting", serial no. [[_____]] 10/675,721, attorney docket no. AUS920030483US1, filed on September 30, 2003; "Method and Apparatus to Autonomically Count Instruction Execution for Applications", serial no. [[_____]] 10/675,642, attorney docket no. AUS920030484US1, filed on September 30, 2003; "Method and Apparatus to Autonomically Take an Exception on Specified Instructions", serial no. [[_____]] 10/675,606, attorney docket no. AUS920030485US1, filed on September 30, 2003; "Method and Apparatus to Autonomically Profile Applications", serial no. [[_____]] 10/675,783, attorney docket no. AUS920030486US1, filed on September 30, 2003; "Method and Apparatus for Counting Instruction and Memory Location Ranges", serial no. [[_____]] 10/675,872, attorney docket no. AUS920030487US1, filed on September 30, 2003; "Autonomic Method and Apparatus for Hardware Assist for Patching Code", serial no. [[_____]] 10/757,171, attorney docket no. AUS920030551US1, filed on [[_____]] January 14, 2004; and "Autonomic Method and Apparatus for Local Program Code Reorganization Using Branch Count Per Instruction Hardware", serial no. [[_____]] 10/757,156, attorney docket no. AUS920030552US1, filed on [[_____]] September 30, 2003. All of the above related applications are assigned to the same assignee, and incorporated herein by reference.--

Please replace the title of the application with the following:

-- AUTONOMIC METHOD AND APPARATUS FOR COUNTING BRANCH INSTRUCTIONS TO GENERATE BRANCH STATISTICS MEANT TO IMPROVE BRANCH PREDICTIONS --

Please replace the paragraphs beginning on page 12, line 27, with the following rewritten paragraphs:

-- In response to a Load instruction, LSU **228** inputs information from data cache **216** and copies such information to selected ones of rename buffers **234** and **238**. If such information is not stored in data cache **216**, then data cache **216** inputs (through BIU **212** and system bus **211**) such information from a system memory [[**239**]] **260** connected to system bus **211**. Moreover, data cache **216** is able to output (through BIU **212** and system bus **211**) information from data cache **216** to system memory [[**239**]] **260** connected to system bus **211**. In response to a Store instruction, LSU **228** inputs information from a selected one of GPRs **232** and FPRs **236** and copies such information to data cache **216**.

Sequencer unit **218** inputs and outputs information to and from GPRs **232** and FPRs **236**. From sequencer unit **218**, branch unit **220** inputs instructions and signals indicating a present state of processor **210**. In response to such instructions and signals, branch unit **220** outputs (to sequencer unit **218**) signals indicating suitable memory addresses storing a sequence of instructions for execution by processor **210**. In response to such signals from branch unit **220**, sequencer unit **218** inputs the indicated sequence of instructions from instruction cache **214**. If one or more of the sequence of instructions is not stored in instruction cache **214**, then instruction cache **214** inputs (through BIU **212** and system bus **211**) such instructions from system memory [[**239**]] **260** connected to system bus **211**. --